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06EC53

Fifth Semester B.E. Degree Examination, Dec.2015/Jan.2016

Analog Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define autocorrelation and explain the physical significance of autocorrelation? **(06 Marks)**

b. If $x(t) = A_c \cos(2\pi f_c t + \theta)$ where A_c and f_c are constant, θ is a random variable that is uniformly distributed over $(-\pi\ \pi)$ there find autocorrelation function and plot it. **(08 Marks)**

c. List the properties of Gaussian process. **(06 Marks)**

2 a. Explain with a neat diagram how square low modulator can be used for generation of AM. **(08 Marks)**

b. Explain Generation of DSBSC using product modulator and demodulation using coherent detector. **(08 Marks)**

c. For $s(t) = 10[\cos 2\pi \times 10^6 t]\ [1 + 0.5\cos 2\pi \times 10^3 t + 0.2 \cos 4\pi \times 10^3 t]$, find total modulated power and net modulation index. **(04 Marks)**

3 a. Derive an expression for SSB modulated signal. **(10 Marks)**

b. Evaluate single tone analysis of SSB signal and detect this signal using coherent detector. **(05 Marks)**

c. Write a note on Quadrature carrier multiplexing. **(05 Marks)**

4 a. Explain generation of VSB using sideband shaping filter. **(08 Marks)**

b. Explain envelop detection of VSB plus carrier wave. **(08 Marks)**

c. Write a note on Frequency Translation. **(04 Marks)**

PART – B

5 a. Derive an expression for spectrum of FM wave with sinusoidal modulation. **(10 Marks)**

b. Explain FM generation using direct method. **(06 Marks)**

c. Define % of modulation and deviation ratio in FM. **(04 Marks)**

6 a. Explain with neat diagram, characteristics and equations, how balanced slope detector can be used for FM demodulation. **(10 Marks)**

b. With the help of neat diagram of Linear model of PLL, show that output is proportional to modulating signal for FM input. **(10 Marks)**

7 a. What is noise figure and equivalent noise temp? Derive an expression for overall Noise figure and equivalent noise temp for cascaded section. **(10 Marks)**

b. Derive an equation for rms noise voltage at the output of passive RC, LPF circuit. **(10 Marks)**

8 a. Obtain an expression for noise in AM receiver using envelop detector. **(08 Marks)**

b. Find figure of merit (FOM) for single tone modulation in FM. **(08 Marks)**

c. Explain briefly Pre-emphasis and De-emphasis. **(04 Marks)**

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10EC56

Fifth Semester B.E. Degree Examination, Dec.2015/Jan.2016
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer FIVE full questions, selecting at least TWO questions from each part.***
2. ***Assume missing data, if any.***

PART – A

1 a. Explain with a neat diagram, enhancement mode transistor action of MOS transistor. **(08 Marks)**

b. Using neat diagram, describe fabrication steps for n-MOS transistor. **(08 Marks)**

c. Compare CMOS and Bipolar technologies. **(04 Marks)**

2 a. What do you mean by Lambda (λ) based design rule? Explain, indicate and draw design rule for PMOS, CMOS and n-mos. **(12 Marks)**

b. Using CMOS logic draw schematic and Layout diagram for $Y = \overline{AB + CD}$. **(08 Marks)**

3 a. Explain why p-MOS and n–MOS has been used in CMOS complementary logic. Discuss CMOS complementary logic with an example. **(06 Marks)**

b. Describe the following logic structures with an example.
i) Pseudo – n-MOS logic
ii) Dynamic CMOS logic **(10 Marks)**

c. Using Bi-CMOS logic structure design a schematic circuit for $h = \overline{ab + c}$. **(04 Marks)**

4 a. What is sheet resistance? Derive the expression for sheet resistance. **(08 Marks)**

b. Explain delay unit. **(06 Marks)**

c. Discuss the scaling factors for n-MOS transistor. **(06 Marks)**

PART – B

5 a. Discuss the architectural issues of CMOS subsystem design. **(04 Marks)**

b. Explain combinational logic using a parity generator. **(08 Marks)**

c. Explain: i) Dynamic register element ii) Dynamic shift register. **(08 Marks)**

6 a. Design and explain 4bit shifter using 4 × 4 cross bar and barrel shifter. **(12 Marks)**

b. Explain with a neat diagram 4 – bit serial – parallel multiplier. **(08 Marks)**

7 a. Explain with a neat diagram, a three transistor dynamic RAM cell. **(08 Marks)**

b. Explain CMOS Pseudo – static memory cell using circuit and stick diagram. **(12 Marks)**

8 a. Discuss the floor plan and layout using 4 – bit processor. **(08 Marks)**

b. Write a short note on
i) Built – in – self – test (BIST)
ii) Scan design technology. **(12 Marks)**

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