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14EVE13

First Semester M.Tech. Degree Examination, Dec.2015/Jan.2016
Advanced Embedded Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Differentiate between RISC and CISC processors. **(04 Marks)**
b. Explain different types of ROM used in an embedded system design. **(08 Marks)**
c. Explain with diagram 7 segment display and LED. **(08 Marks)**

2 a. Explain diagram UART and USB. **(08 Marks)**
b. Explain watchdog timer and reset circuit. **(04 Marks)**
c. Discuss characteristics of an embedded system. **(08 Marks)**

3 a. Explain non operational quality attributes. **(06 Marks)**
b. Explain UML relationship and UML diagrams with examples. **(08 Marks)**
c. Explain dataflow graph and control flow graph. **(06 Marks)**

4 a. What is a printed circuit board? What are different types of PCB and fabrication methods? How can be finished PCB made operational? **(10 Marks)**
b. Explain embedded firmware design approaches. **(10 Marks)**

5 a. Describe the architecture of cortex M3 with neat block diagram. **(10 Marks)**
b. Explain nested interrupts, tail chaining interrupts and late arrival exception handling. **(06 Marks)**
c. Explain memory map of cortex M3 processor. **(04 Marks)**

6 a. Give an overview of nested vector interrupt controller and explain its operation. **(10 Marks)**
b. Explain memory protection unit of cortex M3 and debug architecture of cortex M3. **(10 Marks)**

7 a. Three process ID's P1, P2, P3 with estimated computation time 10, 5, 7 milli seconds respectively enters the ready queue together in the order P1, P2, P3. Calculate the waiting time, turnaround time (TAT) for each process and the average waiting time and turnaround time (assuming there is no I/O waiting for the process). **(06 Marks)**
b. What is deadlock? What are the techniques to detect and prevent deadlock? **(08 Marks)**
c. Explain priority inversion with a neat diagram. **(06 Marks)**

8 a. What is message passing? Give classification for message passing. **(10 Marks)**
b. What are the different hardware debugging tools used in embedded product development? **(05 Marks)**
c. Explain JTAG based boundary scanning for hardware testing. **(05 Marks)**

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